groove extending downward through said third and said second regions into said first region so that a first portion of said third region and a first portion of said second region lie on one side of said first [rectangular] groove and a second portion of said third region and a second portion of said second region lie on the other side of said first [rectangular] groove;

lining said first [rectangular] groove with a dielectric material, thereby forming a second, inner [rectangular] groove;

filling the bottom portion of said second, inner [rectangular] groove with a conductive material so that a top surface of said conductive material in said second, inner groove lies between said first portion and said second portion of said third region, said conductive material serving as a gate; and

forming an insulating layer having a planar top surface over the device resulting from the preceding steps, the thickness of the portion of said insulating layer over said conductive material being greater than the thickness of the portion of said insulating layer over said third region.

~~10.~~ 3. ~~(Amended)~~ A method of making a semiconductor device comprising the following steps:

forming a first region of a semiconductor material having a first conductivity type;

forming a second region of a semiconductor material having a second conductivity type above and in contact with said first region, said second region having a top surface;

forming a third region of said first conductivity

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type in a first portion of said second region, said third region extending to a first portion of said top surface;

forming a first [rectangular] groove in said top surface, and first [rectangular] groove extending downward into said first region so that a portion of said third region and a portion of said second region lies adjacent said first [rectangular] groove on one side of said first [rectangular] groove;

lining said first [rectangular] groove with a dielectric material, thereby forming a second, inner [rectangular] groove;

filling the bottom portion of said second, inner [rectangular] groove with a conductive material so that a top surface of said conductive material in said second, inner groove lies opposite said portion of said third region, said conductive material serving as a gate; and

forming an insulating layer having a planar top surface over the device resulting from the preceding steps, the thickness of the portion of said insulating layer over said conductive material being greater than the thickness of the portion of said insulating layer over said third region.

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12. ~~(Amended)~~ A method for making a semiconductor device comprising the following steps:

providing a first region of semiconductor material having a first conductivity type;

forming a second region of semiconductor material having a second conductivity type above said first region;

forming a third region of said first conductivity type above a portion of said second region;

forming a first groove, said first groove extending

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downward through said third and said second regions into said first region so that a first portion of said third region and a first portion of said second region lie on at least one side of said first groove;

lining said first groove with a dielectric material, thereby forming a second, inner groove;

filling the bottom portion of said second, inner groove but not the top portion of said second inner groove with a conductive material so that the top surface of said conductive material in said second, inner groove lies adjacent to the portion of dielectric material adjacent to said third region, said conductive material serving as a gate; [and]

forming an insulating layer having a planar top surface over the device resulting from the preceding steps, wherein the portion of the insulating layer over said conductive material is thicker than the portion of the insulating layer over said third region;

removing at least a portion of said insulating layer over said third region; and

forming a conductive layer electrically contacting said third region.

Add Claim 17 as follows:

17. A method for making a semiconductor device comprising the steps of:

providing a first region of semiconductor material of a first conductivity type;

forming a second region of semiconductor material of a second conductivity type on said first region;

forming a plurality of semiconductor regions of said

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first conductivity type within said second region;

etching a plurality of grooves so that each groove extends through an associated one of said regions within said plurality of semiconductor regions, through said second region and into said first region;

lining said plurality of grooves with an insulating layer;

filling the bottom portion of said grooves with conductive material, said conductive material serving as a gate;

forming an insulating layer on said conductive material so that the top surface of said semiconductor device is planar; and

electrically contacting the bottom surface of said first region and the top surface of said plurality of semiconductor regions,

wherein said plurality of semiconductor regions, first region, second region, and the conductive material in said plurality of grooves serve as a plurality of cells of a vertical transistor.

B5 cont'd

REMARKS

The Examiner has objected to the specification under 35 USC 112 as failing to provide the best mode of carrying out the invention. Specifically, the Examiner states

> The process of forming gate contact 49 through oxide layer 35 to gate is not described at all. It is not clear from specification page 6, lines 20+ how the applicants fit the contact wire 34 inside the polysilicon filler, and oxidize the top of the filler. Examiner would like to know how the structure of Fig. 7 is obtained from that of Fig. 5, is it by forcing down a metal wire through oxide layer (35) to polysilicon filler.

Applicant respectfully submits that the present specification

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